

Adaptive Serial I/O LIM for Cell or Packet Networks

INTRODUCTION

Xedge Adaptive Serial I/O LIMs (ASIO) operate in Xedge switches to enable transport legacy data over cell or packet networks. These modules support a variety of applications with the Xedge CE, PCX, PCE, PCL or ACP controllers. These arrangements can provide up to four ports of clear channel circuit emulation over Ethernet, or up to four ports of ATM cell switching. When used in conjunction with CE or PCE controllers, ASIO LIMs can transmit bit transparent data encapsulated in cell or Ethernet/IP frames, respectively.

The ASIO LIMs supports both DCE and DTE operation. Each link can be individually configured for DCE or DTE mode through the smart cable connected to it or through the software command when a smart cable is not available.

Timing Options

The ASIO LIM supports several timing options: System Timing, Local Oscillator, Adaptive Clock and External Clock, described below.

- The System Timing reference employs the Xedge6000 timing bus as the system timing source. The ASIO will select which timing bus is used as the 8KHz reference for generating timing on the LIM.
- The Local Oscillator clock reference, located on the ASIO, is an independent clock reference used for generating timing out the ASIO LIM.
- The Adaptive clock reference is from the controller, either the Xedge Circuit Emulation controller or the Xedge Packet Circuit Emulation controller. When the cell/packet "arrival rate" changes, this clock reference will change. In turn, it will trigger the ASIO LIM to adapt to the new clock.
- The External clock option is available when the LIM is configured as a DCE. In this application, the output channel can be selected to use the received clock/ Terminal Timing (TT) as clock reference to output data.

Diagnostics

- Digital Loopbacks loop data and controls (RTS->CTS, DTR->DSR) coming from/to the slot controller.
- Link Loopbacks loop data and controls (RTS->CTS, DTR->DSR) coming from/to the line. All timing signals remain operational.
- Line Loopbacks loop data coming from the line back to the line. Controls are not looped and remain in operational mode. All timing signals remain operational.
- In-progress loopbacks are indicated by front panel LED for each port.

FEATURES & BENEFITS

- Dual and Quad port options
- Adaptive time independent "any speed" circuit emulation
- EIA-530A, EIA-449, ITU-T X.21, ITU-T V.35 and RS-232 interfaces via SCC technology
- High Speed serial interfaces (HSSI or TTL) via the corresponding Mezzanine card
- DTE and DCE operation
- For use with the Xedge Circuit Emulation (CE), Packet Circuit Emulation (PCE), Packet Cell Switch (PCX), Packet Cell Link (PCL) and ACP Controllers
- Used with circuit emulated TDM over packet (Ethernet-IP-MPLS) or TDM over ATM
- System, External, Adaptive or Local Oscillator timing
- Per port In Service and Loopback LEDs on the LIM, controlled by the state of the slot controller
- Data rates from 75 bps to 51.82 Mbps

Xedge ASIO Models

- The standard model of the 4-port ASIO LIM supports EIA-530A, EIA-449, ITU-T X.21, ITU-T V.35 and RS-232 interfaces by means of a Smart Cable at each of the miniature 26-pin high density connectors.
- The ASIO-HSSI LIM (DCE) LIM supports the ECL protocol at each of its 50-pin ports up to 51.82 Mbps.

Future ASIO Models

The Xedge family of ASIO LIMs also includes ASIO-TTL and ASIO-HSSI (DTE), planned as future models:

- The ASIO-TTL (2-port or 4-port) supports the higher speed TTL interface at each pair of its BNC connectors.
- The ASIO-HSSI DTE LIM (2-port) supports the higher speed ECL protocol at each of its 50-pin ports.

Data Rates

The standard ASIO LIM supports programmable data rates from 75 bps up to 10 Mbps in increments of 1 bps. The ASIO-TTL and both ASIO-HSSI models are designed to support programmable data rates from 75 bps up to 51.82 Mbps in increments of 1 bps.

For all ASIO LIMs in adaptive mode, the data rate automatically adjusts to incoming stream arrival time.

Xedge ASIO LIMs

SAMPLE APPLICATIONS

The ASIO is intended for use in a variety of applications, including the transport of telemetry data for aerospace and defense, as well as real time SCADA information for utilities and industrial applications. The ASIO can flexibly support multiple data rates from very low to high speed, and operates with Xedge controller modules for the transport of TDM bit transparent data over an ATM or Ethernet/MPLS network.

In addition to its function as a user interface for data acquisition, an ASIO LIM can also serve as a network trunk interface to transport multi-service data, for example, over satellite.

Figure 1 shows the ASIO supporting the acquisition of TDM data using either the Packet Circuit Emulation (PCE) controller or the Circuit Emulation controller to encapsulate bits-transparent TDM into Ethernet/IP or ATM cells, respectively. Figure 1 also illustrates one of the several timing options of the ASIO; in this case system timed for synchronous transmission.

Figure 2 also shows user side acquisition of serial TDM data but where in Figure 1 the timing scheme is a system reference clock from Xedge, Figure 2 employs an adaptive timing scheme from the clock on the CE or PCE as the controller. The controller adapts to the arrival rate of cells or packets dynamically, depending on such factors as vehicular movement of objects from which data is acquired.

Figure 1: Circuit Emulation over Packet or ATM with Xedge-supplied clock.

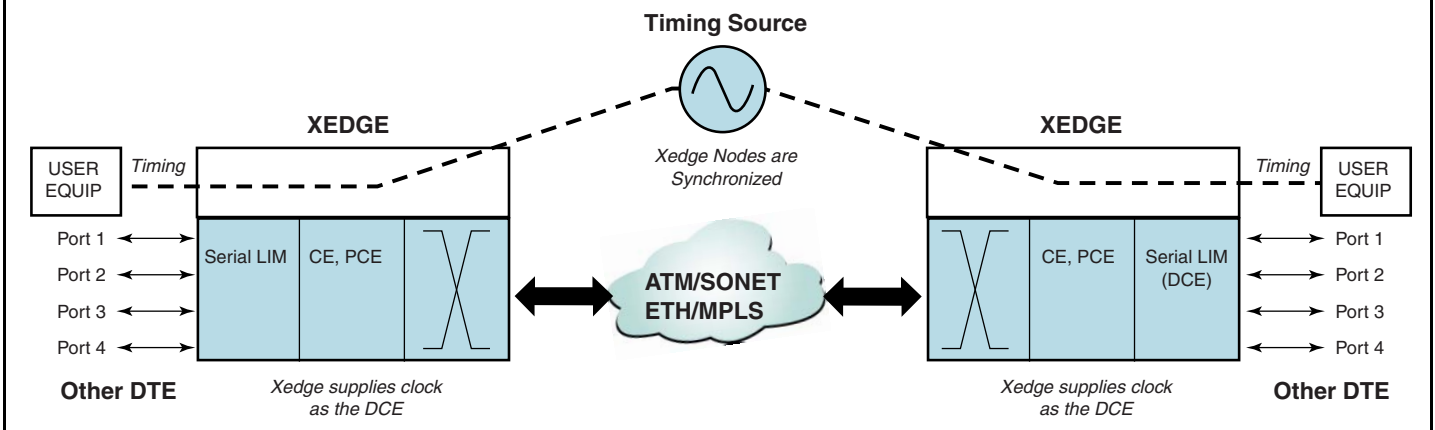
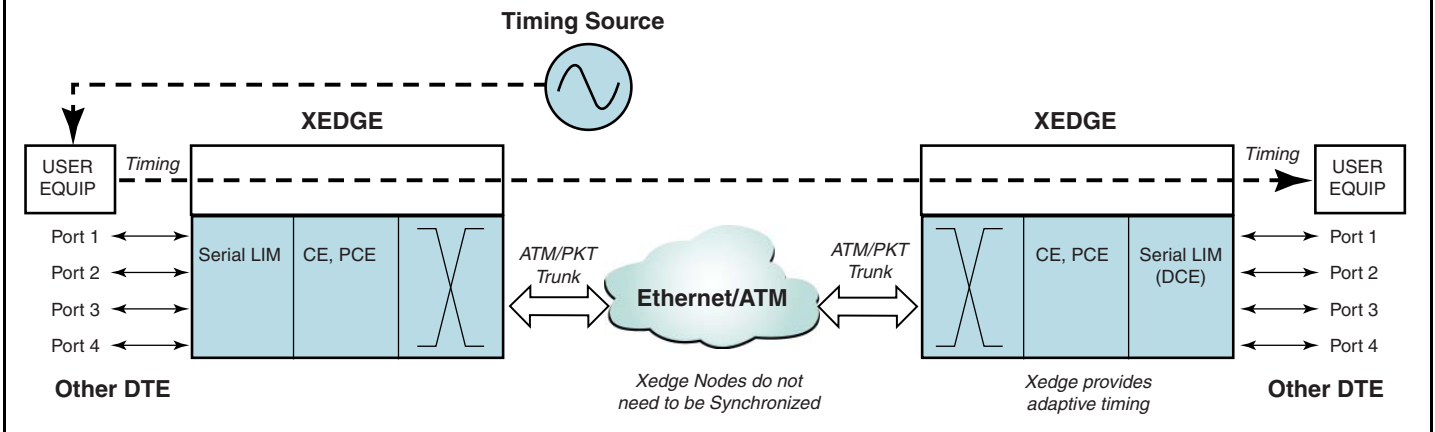


Figure 2: Circuit Emulation over Packet or ATM with Adaptive Timing



Xedge ASIO LIMs

Figure 3 illustrates the use of the ASIO LIM for clock tracking. The Doppler effect of the clock received from the airborne vehicle can be tracked, as well as the changes in the application's clock rate.

Figure 4 illustrates the flexibility of ASIO timing options. Scenario A shows the ASIO LIM using the system bus as the timing source; Scenario B shows the system bus using the ASIO LIM as a source for the system clock.

Figure 3: Clock Tracking via the ASIO

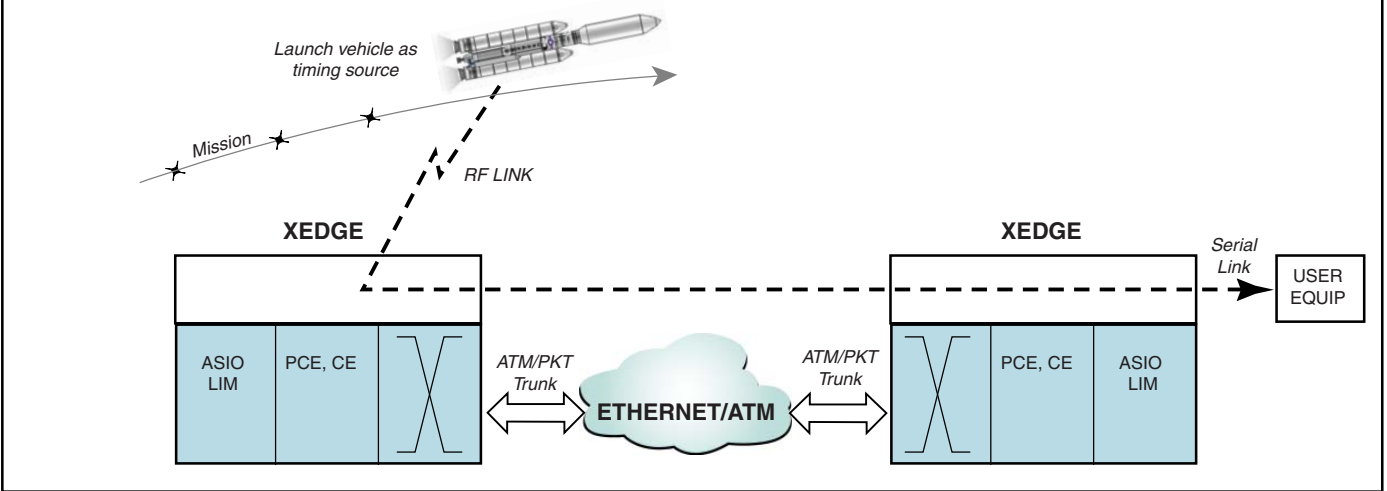


Figure 4A: Timing Options

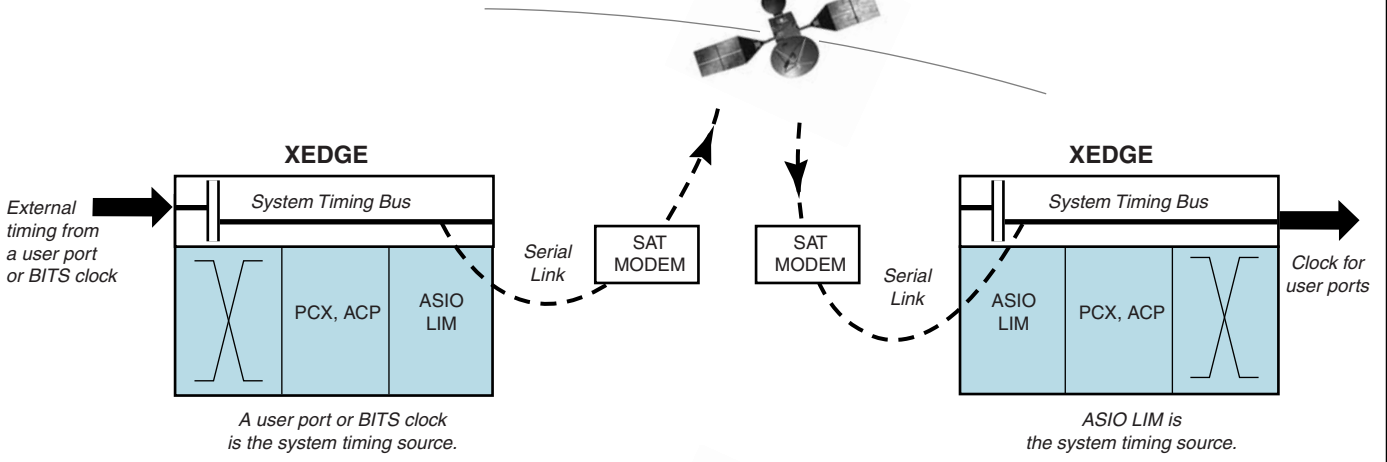
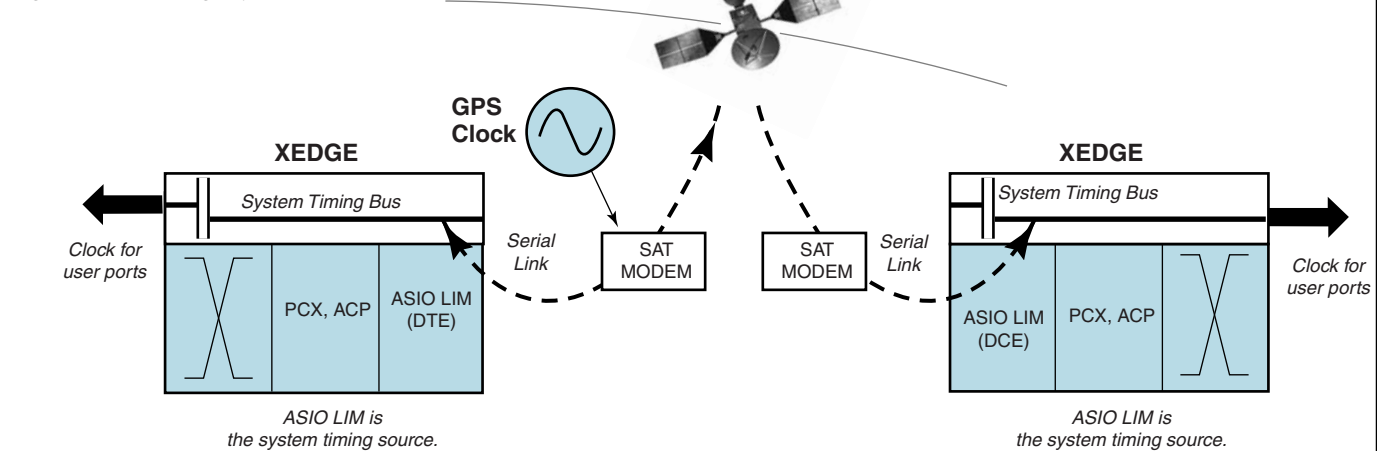


Figure 4B: Timing Options



Xedge ASIO LIMs

Specifications

LIM Models/Supported Interfaces

Xedge ASIO (standard) supports EIA-530A, EIA-449, ITU-T X.21, ITU-T V.35, and RS-232 up to 4 ports via Smart Cable Connectors.

Xedge ASIO-HSSI supports ECL up to 2 ports.

Xedge ASIO-TTL supports TTL up to 4 ports.

Operational Specifications (all models)

Compatible Controllers: CE, PCE, PCX, PCL, ACP

Compatible Chassis: Xedge 6002, 6160, 6280, 6640 and 6645

Port Capacity: up to 4 ports, depending on the LIM model and/or the LIM/controller

Operation: Simplex, Duplex, Asymmetrical

Alarms: Loss of Signal, No System Clock

Timing Modes: System, External, Adaptive, Local Oscillator on LIM

Network Management: SNMP

Operating Temperature: 0 to 50 degrees C.

Storage Temperature: -40 to 70 degrees C.

Humidity: Up to 95 percent, non-condensation

Dimensions: 10.5" x 8" x 1"

Weight: Approximately 1 lb.

Data Rates

LIM Type	Controller	# ports	Speeds Per Port
ASIO (Standard)	CE	2/4 ports	From 2.4 to 8,192 Kbps, plus custom rates
	ACP	2 ports	Up to 10 Mbps per port
	PCE	4 ports	Up to 4.65 Mbps per port, 9.3 Mbps total all ports
		2 ports	Up to 10 Mbps per port
PCX/2	2 ports	Up to 10 Mbps per port	
ASIO-HSSI (DCE)	CE	2 ports	(TBD)
	ACP	2 ports	Up to 51.82 Mbps
	PCE	2 ports	Up to 51.82 Mbps
	PCX/2	2 ports	Up to 51.82 Mbps
ASIO-TTL (Future)	CE	2/4 ports	(TBD)
	ACP	2 ports	
	PCE	2/4 ports	
	PCX/2	2 ports	
ASIO-HSSI (DTE) (Future)	CE	2 ports	(TBD)
	ACP, PCE, and PCX/2	2 ports	Up to 51.82 Mbps

Note: Data rates are adjustable in 1 bps increments.

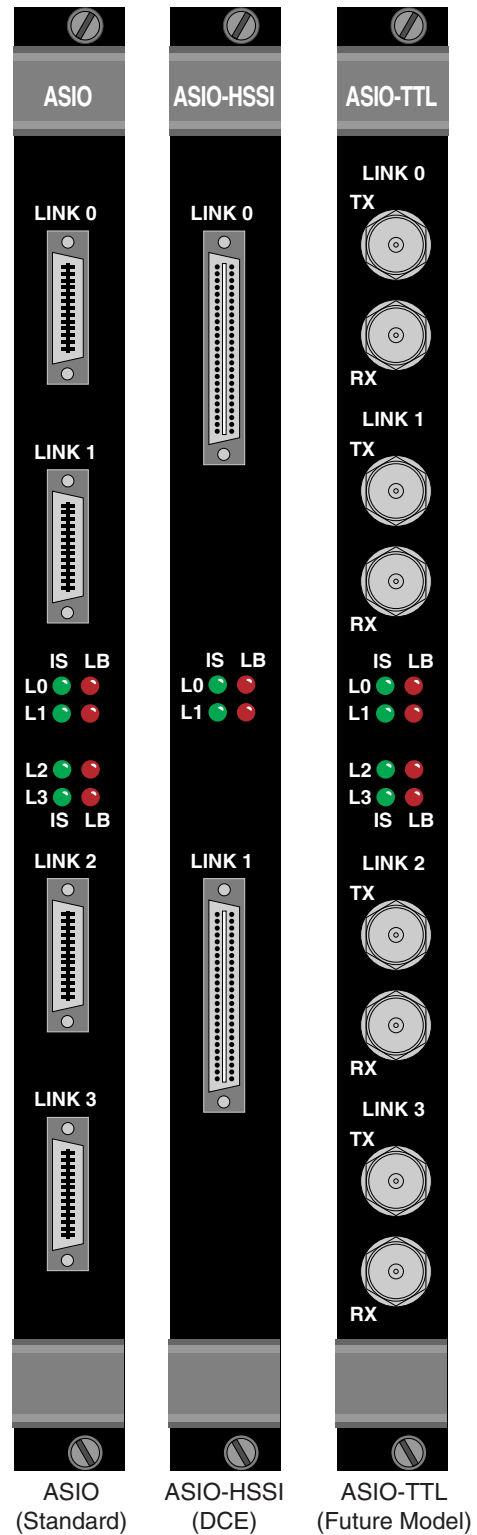


Figure 5: Front Panel Views of Xedge family of ASIO LIMs